I claim:

1. A memory cell, comprising:

a vertical access device including a selective epitaxy mesa; and

a storage device on the selective epitaxy mesa.

2. The memory cell of claim 1, wherein selective epitaxy mesa includes a bottom source/drain and a top source/drain, and wherein the selective epitaxy mesa further includes a conductive body separating the bottom source/drain from the top source/drain.

3. The memory cell of claim 2, wherein the bottom source/drain is an in situ doped region.

4. The memory cell of claim 2, wherein the top source/drain is an in situ doped region.

5. The memory cell of claim 2, wherein the bottom source/drain includes a semi-annular ring around a bottom portion of the selective epitaxy mesa.

6. The memory cell of claim 5, wherein the vertical access device includes a signal line having a first height, and wherein the bottom source/drain includes a second height that is about equal to the first height.

7. The memory cell of claim 5, wherein the bottom source/drain is formed by out diffusion from an adjacent conductor.

8. The memory cell of claim 1, wherein the access device is free from a shallow trench isolation layer.

9. A vertical memory cell, comprising:

a substrate;

an access device including a selective epitaxy mesa formed on and extending outwardly from the substrate; and

a storage device on the selective epitaxy mesa.

10. The memory cell of claim 9, wherein the substrate includes silicon, and wherein the selective epitaxy mesa includes silicon.

11. The memory cell of claim 9, wherein the access device includes a body, a first source/drain, a gate and a second source/drain, wherein the body extends between the first source/drain and the second source/drain, and wherein the first source/drain and the second source/drain are each a selective epitaxy doped region of the selective epitaxy mesa.

12. The memory cell of claim 11, wherein the first source/drain region extends horizontally around the selective epitaxy mesa.

13. The memory cell of claim 12, wherein the first source/drain region is adapted to contact a bit line.

14. The memory cell of claim 12, wherein the second source/drain region is spaced from the substrate by the body.

15. The memory cell of claim 14, wherein the second source/drain region is an in situ N+ doped region of the selective epitaxy mesa.

16. A vertical memory cell, comprising:

a substrate;

an electrical signal line on the substrate;

an access device including a selective epitaxy mesa formed on and extending outwardly from the substrate, the selective epitaxy mesa including a first source/drain region adjacent the substrate and in electrically communication with the electrical signal line; and

a storage device on the selective epitaxy mesa.

17. The vertical memory cell of claim 16, wherein the electrical signal line has a first height, and wherein the first source/drain region has a second height equal to or less than the first height.

18. The vertical memory cell of claim 16, wherein the selective epitaxy mesa cantilevers upwardly from the substrate, and wherein the selective epitaxy mesa includes an end, remote from the substrate, forming a second source/drain region.

19. The vertical memory cell of claim 16, wherein the first source/drain region extends around an outer periphery of the selective epitaxy mesa.

20. The vertical memory cell of claim 19, wherein the electrical signal line extends around the first source/drain region.

21. The vertical memory cell of claim 16, wherein the first source/drain region extends partially around an outer periphery of the selective epitaxy mesa.

22. The vertical memory cell of claim 21, wherein the electrical signal line extends around the first source/drain region.

23. The vertical memory cell of claim 21, wherein the electrical signal line partially around the selective epitaxy mesa.

24. The vertical memory cell of claim 16, wherein the first source/drain region is adapted to electrically communicate with a column address decoder through a buried bit line.

25. The vertical memory cell of claim 24, wherein the second source/drain region is adapted to electrically communicate with the storage device.

26. A vertical memory cell, comprising:

a substrate;

an electrical signal line on the substrate;

an access device including a selective epitaxy mesa formed on and extending outwardly from the substrate, the selective epitaxy mesa including a first source/drain region adjacent the substrate and in electrically communication with the electrical signal

line, the selective epitaxy mesa further including a body extending vertically from the first source/drain region, an insulator on the body, and a gate on the insulator; and

a storage device on the selective epitaxy mesa remote from the substrate.

27. The vertical memory cell of claim 26, wherein the insulator surrounds the body, and wherein the gate surrounds the insulator such that the gate effects electrical conductivity of the body from more than one angle.

28. The vertical memory cell of claim 26, wherein the insulator surrounds the body, and wherein the gate partially overlies the insulator such that the gate effects electrical conductivity of the body from more than one angle.

29. The vertical memory cell of claim 28, wherein the gate overlies over half of a surface area of the body.

30. The vertical memory cell of claim 26, wherein the electrical signal line includes titanium.

31. A vertical transistor, comprising:

a vertical, selective epitaxy body extending from a horizontal substrate;

a first doped region in the body adjacent the substrate;

a second doped region in the body remote from the substrate;

an undoped intermediate region between the first doped region and the second doped region; and

a gate at least partially surrounding the intermediate region.

32. The transistor of claim 31, wherein the body is adapted to form a channel between the doped first region and the doped second region.

33. The transistor of claim 31, wherein the first doped region is adapted to be in electrically communication with a buried bit line.

34. The transistor of claim 31, wherein the gate is adapted to be in electrical communication with a word line.

35. The transistor of claim 31, wherein the gate overlies at least half of the surface area of the intermediate region.

36. The transistor of claim 31, wherein the gate overlies at least about 75% of the surface area of the intermediate region.

37. The transistor of claim 31, wherein the gate overlies about all of the surface area of the intermediate region.

38. The transistor of claim 31, wherein the vertical, selective epitaxy body is generally cylindrical.

39. The transistor of claim 38, wherein the gate is generally annular and extends completely around the body.

40. The transistor of claim 38, wherein the first doped region is cylindrical.

41. A method of fabricating an integrated circuit device, comprising:

patterning a buried conductor line on a substrate;

forming recess through the buried conductor line to the substrate;

forming, through selective epitaxy, a vertical mesa in the recess;

doping a first source/drain region in electrical communication with the buried conductor while forming the mesa;

forming a gate oxide on the mesa;

forming a gate on the gate oxide at least partially surrounding the mesa; and

forming a second source/drain region at a top of the mesa remote from the substrate.

42. The method of claim 41, wherein doping a first source/drain region includes forming an ohmic contact with the buried layer, which forms a buried bit line.

43. The method of claim 42, wherein doping a first source/drain region includes forming the first source/drain region at a vertical dimension about equal or less than the buried bit line.

44. The method of claim 41, wherein forming a second source/drain region includes further selective epitaxially growing a doped region on the mesa.

45. The method of claim 41, wherein forming a second source/drain region includes further selective epitaxially growing a region on the mesa and thereafter doping the region.

46. The method of claim 45, wherein doping the region includes thermally driving a dopant into the region.

47. The method of claim 41, wherein doping, by out-diffusion, the first source/drain region includes forming the first source/drain region around the outer periphery of the mesa.

48. The method of claim 41, wherein doping a first source/drain region includes doping a region of the mesa to a height generally equal to a height of the buried conductor line.

49. The method of claim 48, wherein doping a first source/drain region includes completely enclosing the first source/drain region with the buried conductor line.

50. The method of claim 48, wherein forming recess through the buried conductor line to the substrate includes forming the recess through an insulative layer on the buried conductor line.

51. The method of claim 50, wherein forming recess through the buried conductor line to the substrate includes forming the recess through a further insulative layer intermediate the buried conductor line and the substrate.

52. The method of claim 41, wherein forming, through selective epitaxy, a vertical mesa includes using chemical vapor deposition processes that are adapted for selective epitaxy.

53. A method of fabricating an integrated circuit device, comprising:

patterning a buried conductor line on a substrate;

forming recess through the buried conductor line to the substrate;

forming, through selective epitaxy, a vertical mesa in the recess;

doping a first source/drain region in electrical communication with the buried conductor while forming the mesa;

forming a gate oxide on the mesa;

forming a gate on the gate oxide at least partially surrounding the mesa; and

doping, while forming the mesa, a second source/drain region at a top of the mesa remote from the substrate.

54. The method of claim 53, wherein patterning the buried conductor includes connecting the buried conductor line to a memory decoder for a memory device.

55. The method of claim 53, wherein doping a first source/drain region includes doping the mesa with N type dopants.

56. The method of claim 53, wherein forming, through selective epitaxy, a vertical mesa includes performing homoepitaxy of silicon.

57. The method of claim 54, wherein performing homoepitaxy of silicon includes exposing a silicon surface to a gas mixture including H_2 and SiH_2Cl_2 in a temperature range between 600-800 degrees C.

58. The method of claim 53, wherein forming, through selective epitaxy, a vertical mesa includes exposing the recess to a gas mixture having GeH_4.

59. The method of claim 53, wherein forming, through selective epitaxy, a vertical mesa includes using a molecular beam epitaxy.

60. The method of claim 59, wherein using a molecular beam epitaxy includes using a gas source.

61. The method of claim 53, wherein forming, through selective epitaxy, a vertical mesa includes depositing silicon atoms produced by a gas phase reaction striking one of a silicon substrate surface or a previously deposited selective epitaxy film.

62. The method of claim 61, wherein depositing silicon atoms includes providing at least one of silicon tetrachoride ($SiCl_4$), silane (SiH_4), dichlorosilane (SiH_2Cl_4 or DCS), trichlorosilane (TCS), or other hydrogen reduced chlorosilanes (SiH_xCl_{4-x}).

63. The method of claim 53, wherein forming the mesa includes forming a body that has a height greater than a cross sectional dimension.

64. A method for fabricating an integrated circuit device including a transistor, comprising:

patterning a buried conductor line on a substrate;

forming recess through the buried conductor line to the substrate;

forming, through selective epitaxy, a vertical mesa in the recess;

doping a first source/drain region in electrical communication with the buried conductor while forming the mesa;

forming a second source/drain region at a top of the mesa remote from the substrate;

forming a gate oxide layer on the substrate and the mesa;

forming a gate layer on the gate oxide at least partially surrounding the mesa;

forming an insulative layer on the gate layer; and

planarizing the gate oxide layer, the gate layer and the insulative layer off the top of the mesa.

65. The method of claim 64, wherein forming a second source/drain region is performed after planarizing.

66. The method of claim 65, wherein forming an insulative layer includes filling the gaps between the vertical mesas and insulative layers with a further insulative material.

67. The method of claim 64, wherein patterning a buried conductor line includes forming a first insulative layer on the substrate, masking the insulative layer, patterning the buried conductive layer using the masking; and covering the patterned buried conductive layer with a second insulative layer.

68. The method of claim 67, wherein forming the recess includes forming the recess through the first insulative layer, the buried conductive layer, and the second conductive layer to reach the substrate.

69. A method for fabricating an integrated circuit device including a memory cell, comprising:

patterning a buried conductor line on a substrate;

forming recess through the buried conductor line to the substrate;

forming, through selective epitaxy, a vertical mesa in the recess;

doping a first source/drain region in electrical communication with the buried conductor while forming the mesa;

forming a second source/drain region at a top of the mesa remote from the substrate;

forming a gate oxide layer on the substrate and the mesa;

forming a gate layer on the gate oxide at least partially surrounding the mesa;

forming an insulative layer on the gate layer;

planarizing the gate oxide layer, the gate layer and the insulative layer off the top of the mesa; and

forming a memory structure on the second source/drain region.

70. The method of claim 69, wherein forming the gate layer includes extending the gate layer completely around the periphery of a portion of the mesa.